BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

TELEPHONE: (303) 740-1980

INTELLECTUAL PROPERTY LAW
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

FACSIMILE: (303) 740-6962

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Deliver to: Mai, Tan V., USPTO
Art Group: 2193
Facsimile No.: (571) 273-8300
Date: September 10, 2007
From: Brent E. Vecchia, Reg. No. 48,011
Our Docket No.: 42P14609
Number of pages 31 including this sheet.
Application No.: 10/658,612
Filing Date: 9/8/2003
Docket Due Date(s): 9/10/2007

Enclosed are the following documents:

☐ Amendment: (pgs)	☐ Issue Fee Transmittal
☒ Appeal Brief (27 pgs)	☐ Notice of Appeal (in duplicate)
☐ Application:	☐ Petition for:
(27 pgs) w/cover & abstract)	☐ Request for Continued Examination (RCE)
☐ Assignment & Cover Sheet (pgs)	☐ Reply Brief (pgs)
☒ Certificate of Facsimile	☐ Request & Certification Under 35 USC 122(b)(2)(B)(i)
☐ Continued Prosecution Application (CPA)	☐ Request to Rescind Previous Nonpublication Request
☐ Declaration & POA (pgs)	☐ Response to Notice of Missing Parts & Formalities Letter
☐ Drawings: sheets, figures	☐ Response to Written Opinion (pgs)
☐ Extension of Time:	☐ Terminal Disclaimer
☒ Fee Transmittal (in duplicate)	☐ Transmittal of Publication Fee Due
☐ IDS & PTO/SB/08 (pgs)	☒ Transmittal Letter
☐ Other:	

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	10/658,612
Filing Date	September 8, 2003
First Named Inventor	Gopalan Ramanujam
Art Unit	2193
Examiner Name	Mai, Tan V.
Total Number of Pages in This Submission	31
Attorney Docket Number	42P14609

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Other Enclosure(s) *(please identify below):*

Facsimile Cover Sheet

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Brent E. Vecchia, Reg. No. 48,011 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Brent E. Vecchia
Date	September 10, 2007

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FEE TRANSMITTAL for FY 2006

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	10/658,612
Filing Date	September 8, 2003
First Named Inventor	Gopalan Ramanujam
Examiner Name	Mai, Tan V.
Art Unit	2193
Attorney Docket No.	42P14609

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20. ☒ Credit any overpayments

FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) ($) 500.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Brent E. Vecchia	Registration No. (Attorney/Agent)	48,011	Telephone	(303) 740-1980
Signature	Brent E. Vecchia			Date	09/10/07

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application. No.	: 10/658,612	Confirmation No.	: 2531
1st Named Inventor	: Gopalan Ramanujam	Art Unit	: 2193
Filed	: 09/08/2003	Examiner	: Tan V. Mai
Docket No.	: 42P14609	Customer No.	: 7590

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Alexandria, VA 22313-1450

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

This brief is in furtherance of the Notice of Appeal, filed in the above-captioned case on 7/10/2007. Applicants (hereafter "Appellants") hereby submit this Brief (37 C.F.R. § 41.37). The fees required under § 41.20(b)(2), and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying Transmittal of Appeal Brief. Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

An oral hearing is not desired.

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TABLE OF CONTENTS

This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37c(1)):

Page 18 of this brief bears the practitioner's signature.

I. REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California, 95052, to whom the invention is assigned.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c)(1)(ii))

With respect to other appeals or interferences that will directly affect, or be affected by, or have a bearing on the Board's decision in this appeal, to the best of Appellant's knowledge, there are no such appeals or interferences.

III. STATUS OF THE CLAIMS (37 C.F.R. § 41.37(c)(1)(iii))

The status of the claims in this application are:

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims 1-33 are currently pending in the application.

B. STATUS OF ALL THE CLAIMS

1. Claims cancelled: NONE
2. Claims withdrawn from consideration but not cancelled: NONE
3. Claims pending: 1-33
4. Claims allowed: 26-31.
5. Claims rejected: 1-25 and 32-33

C. CLAIMS ON APPEAL

Claims 1-25 and 32-33 are on appeal.

IV. STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

A response was submitted in response to the Final Office Action on 5/25/2007. However the response did not contain amendments to the claims or to the other parts of the specification. As understood by Appellant, the Examiner has elected to enter the amendments (which there are none). A copy of all claims on appeal is attached hereto as an appendix of claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

Embodiments of the invention pertain to a method, apparatus, and instructions, for parallel data conversion. See e.g., the Title.

Independent claim 1 pertains to an apparatus according to a first embodiment of the invention. See e.g., original claim 1. The apparatus includes a destination storage location corresponding to a first architectural register. See e.g., register file 122 in FIG. 1, paragraph [0028], and destination register 320 in FIG. 3a. The apparatus also includes a functional unit. See e.g., functional unit 130 in FIG. 1, paragraph [0031], execution units 255-1 through 255-N in FIG. 2a. The functional unit is to process a packed format values (see e.g., paragraph [0030]) by converting, responsive to a control signal (see e.g., paragraph [0031]; control signal as indicated by arrow 135 in FIG. 1). For the following, see e.g., paragraph [0032] and paragraphs [0044] through [0047]. A first packed first format value (see e.g., B1G1R1A1 in 310 of FIG. 3a) in a first format selected from a first plurality of packed first format values in the first format to a first plurality of second format values (see e.g., packed data elements B1, G1, R1, A1 in 320 of FIG. 3a). The first packed first format value having a plurality of sub elements (see e.g., B1G1R1A1 in 310 of FIG. 3a) each having a first number of bits. Each of the first plurality of second format values being a number represented in a second format and having a second number of bits which is greater than the first number of bits. See e.g., paragraphs [0044] and [0046]. The functional unit to store all of said first plurality of second format values into said first architectural register. See e.g., destination register 320 in FIG. 3a. Other examples of apparatus, according to various embodiments, are shown and described in conjunction with FIGs. 3b, 6, 7a, and 8a.

Independent claim 15 pertains to an apparatus according to a second embodiment of the invention. See e.g., original claim 15. The apparatus includes a decoder. See e.g., decoder 220 in FIG. 2a and paragraph [0035]. The decoder to receive a first instruction and to decode said

first instruction into a control signal (see e.g., paragraph [0031] and second control signal as indicated by arrow 140). The apparatus also includes a functional unit (see e.g., functional unit 130 in FIG. 1, paragraph [0031], and execution units 255-1 through 255-N in FIG. 2a) coupled to the decoder. The functional unit to receive the control signal. See e.g., paragraph [0031] and second control signal as indicated by arrow 140. For the following, see e.g., paragraphs [0049] through [0050], and FIGs. 4a and 4b. The functional unit to responsively process a plurality of floating point values value (see e.g., packed data elements B1, G1, R1, A1 in 410 of FIG. 4a) by converting convert a first plurality of floating point values in a first floating point format having a first number of bits into a first integer value comprising a plurality of sub elements (see e.g., B1G1R1A1 in 420 of FIG. 4a). Each of the sub elements having a second number of bits less than the first number of bits. See e.g., paragraphs [0044] and [0046]. The functional unit to store said first integer value in a first position in a first register, the first register being capable of storing a plurality of integer values in a plurality of individually accessible positions. See e.g., destination register 420 in FIG. 4a. Other examples of apparatus, according to various embodiments, are shown and described in conjunction with FIGs. 4a, 4b, 5, 7b, and 8b.

Independent claim 20 pertains to a method according to a third embodiment of the invention. See e.g., original claim 20. The method includes a module fetching a first instruction. See e.g., paragraphs [0041] and [0069]. The instruction specifies a location of a first format value in a first format among a plurality of first format values of a packed data. See e.g., paragraph [0047]. For the following, see e.g., paragraph [0032] and paragraphs [0044] through [0047]. The first format value having a plurality of sub elements (see e.g., B1G1R1A1 in 310 of FIG. 3a) each sub element having a first number of bits. A functional unit processing the first format value by converting the first format value to a first plurality of second format values in a second format (see e.g., packed data elements B1, G1, R1, A1 in 320 of FIG. 3a). Each of the first plurality of second format values having second format and corresponding to one of the plurality of sub elements. See e.g., the correspondence in FIG. 3a. The second format having a

multiple of the first number of bits. See e.g., paragraphs [0044] and [0046]. Storing the first plurality of second format values into a first register. See e.g., destination register 320 in FIG. 3a. Other examples of the method, according to various embodiments, are shown and described in conjunction with FIGs. 3b, 6, 7a, and 8a.

Independent claim 32 pertains to a tangible machine readable medium according to a fourth embodiment of the invention. See e.g., original claim 32 and paragraph [0069]. The medium carrying an instruction, which if executed by a machine, causes the machine to perform operations. See e.g., original claim 32 and paragraph [0069]. For the following, see e.g., paragraph [0032] and paragraphs [0044] through [0047]. The operations include converting an integer value (see e.g., B1G1R1A1 in 310 of FIG. 3a), the integer value being among a plurality of integer values of a packed data and having a first integer format having a plurality of sub elements (see e.g., B1G1R1A1 in 310 of FIG. 3a) each having a first number of bits. The conversion is to a plurality of floating point values (see e.g., packed data elements B1, G1, R1, A1 in 320 of FIG. 3a). Each of the plurality of floating point values having a first floating point format, the first floating point format having a multiple of the first number of bits. See e.g., paragraphs [0044] and [0046]. The operations also include storing the plurality of floating point values into a first register. See e.g., destination register 320 in FIG. 3a. Other examples of operations, according to various embodiments, are shown and described in conjunction with FIGs. 3b, 6, 7a, and 8a.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

A. Claims 1-25 and 32-33 are rejected under 35 U.S.C. § 101 because the claimed invention is allegedly directed to non-statutory subject matter

VII. ARGUMENT (37 C.F.R. § 41.37(c)(1)(vii))

A. Rejection of claims 1-25 and 32-33 under 35 U.S.C. § 101 is improper

GROUP I: CLAIMS 1-19

Initially, a brief review may be helpful. As discussed in MPEP 2106 IV. C., "*While abstract ideas, natural phenomena, and laws of nature are not eligible for patenting, methods and products employing abstract ideas, natural phenomena, and laws of nature to perform a real-world function may well be. In evaluating whether a claim meets the requirements of section 101, the claim must be considered as a whole to determine whether it is for a* ***particular application*** *(emphasis added) of an abstract idea, natural phenomena, or law of nature, and not for the abstract ideal, natural phenomenon, or law of nature itself.*"

Further, as discussed in MPEP 2106 IV. C. 2., "*For claims including such excluded subject matter to be eligible for patent protection, the claim must be for a* ***practical application*** *(emphasis added) of the abstract idea, law of nature, or natural phenomenon.*" Furthermore, "*A claimed invention is directed to a practical application of a 35 U.S.C. 101 judicial exception when it: (A) 'transforms' an article or physical object to a different state or thing; or (B)* ***otherwise produces a useful, concrete and tangible result***" (emphasis added). See also e.g., MPEP 2106 IV. C. 2. (2).

Claim 1 pertains to an apparatus comprising:

"*a destination storage location corresponding to a first architectural register:*

a functional unit to process a packed format values by converting, responsive to a control signal, a first packed first format value in a first format selected from a first plurality of packed first format values in the first format to a first plurality of second format values, said first packed first format value having a plurality of sub elements each having a first number of bits, each of the first plurality of second format values being a number represented in a second format and having a second number of bits which is greater than the first number of bits, said functional unit to store all of said first plurality of second format values into said first architectural register."

(a) Firstly, Appellants respectfully submit that claim 1 produces a useful, concrete, and tangible result, and is therefore statutory.

On page 3 of the Office Action mailed 4/12/2007, the Examiner has admitted that the result "*would appear to be **concrete** and **tangible** in the context of the claim*". Appellants respectfully agree.

However, the Examiner has asserted that "*the **useful** result appears lacking*". See e.g., page 3 of the Office Action mailed 4/12/2007. Appellants respectfully disagree. Claim 1 does produce a useful result. As one example, the result produced by claim 1 is useful for pixel processing.

As discussed in paragraph [0002], "*As computer and other processing systems handle larger amounts of video or image data, techniques to expedite such processing grow in importance*". As discussed in paragraph [0004], "*Processing of pixels may be performed in formats other than their pixel (e.g., integer) representation. For example, to perform some mathematical operations on pixel values, conversion to a floating point representation first may be desirable*". As discussed in paragraph [0005], "*If the processing device does not offer instructions to efficiently process values such as pixel values, then it may be difficult to construct an efficient software sequence*".

As discussed in paragraph [0026], "*The present disclosure details various conversion and processing techniques that may be advantageous for some types of data in some environments. For example, image processing and particularly pixel processing may be expedited using disclosed techniques in some cases*". As discussed in paragraph [0033], "*It may be advantageous to break down a set of smaller sub elements in a first format into the same number of elements in a more expanded or detailed format in a variety of applications. For example, pixel data may comprise a number of components but pixels may be generally manipulated or moved as a unit. Therefore, elements A, B, C and D in register 125 may be individual pixels. It*

may be advantageous to manipulate the sub elements of these pixels. Therefore, a convert operation according to disclosed techniques can be used to extract the pixel sub element (component) information for further processing in another format. Performing the conversion of all of the individual sub elements of a pixel in response to a single control signal may greatly expedite pixel processing sequences in some cases."

Figures 3A-8B illustrate conversions performed according to various embodiments using RGB & A labels for the data sub elements to indicate that the data may be the red, green, blue, and alpha components of a pixel. See e.g., paragraph [0045].

As shown in Figure 10, and discussed in paragraph [0073], "*As indicated in block 1040, floating point operations may be performed on the pixel values. A great variety of different pixel manipulation techniques are known to those of skill in the art. An appropriate routine depends on the effect that is sought as will be apparent to those of skill in the art. However, the conversion process to and from floating point may be accomplished more efficiently using disclosed techniques*".

Accordingly, the result produced by claim 1 is useful at least for pixel processing.

The result produced by claim 1 is also useful to provide shorter and in some case more rapidly executed code for some sequences. See e.g., paragraph [0076].

The result produced by claim 1 is also useful for signal processing scenarios. For example, as discussed in paragraph [0026], "*Additionally, it is anticipated that disclosed conversion techniques may find applicability in a wide variety of signal processing scenarios and/or in many different processing environments*".

Accordingly, for at least one or more of these reasons, Appellants respectfully submit that claim 1 produces a useful, concrete, and tangible result, and is therefore statutory.

(b) Secondly, Appellants respectfully submit that claim 1 pertains to an apparatus having "*specific structural limitations*", and is therefore statutory.

Appellants respectfully submit that claim 1 is directed to a specialized apparatus having "*specific structural limitations*" and specific interactions between the structural elements. For example, claim 1 recites an apparatus comprising "*a destination storage location corresponding to a first architectural register*" and a specific "functional unit". The specific functional unit is "*to process a packed format values by converting, responsive to a control signal,*" and "*to store all of said first plurality of second format values into said first architectural register*".

As understood by Appellants, a claimed invention including "specific structural limitations" or a specific apparatus is **statutory** (emphasis added). See e.g., *In re* Iwahashi, 888 F.2d 1370, 12 USPQ 2d 1908 (Fed. Cir. 1989).

Furthermore, as stated in MPEP 2106.IV.B.2, "*If a claim defines a useful machine or manufacture by identifying the physical structure of the machine or manufacture in terms of its hardware or hardware and software combination, it **defines a statutory product*** (emphasis added)". See e.g., *Lowry*, 32 F.3d at 1583, 32 USPQ2d at 1034-35; *Warmerdam*, 33 F.3d at 1361-62, 31 USPQ2d at 1760.

Still further, as stated in MPEP 2106.IV.B.2, "*A claim limited to a machine or manufacture, which has a practical application in the technological arts, is statutory (emphasis added). In most cases, a claim to a specific machine or manufacture will have (emphasis added) a practical application in the technological arts*". See *Alappat*, 33, F.3d at 1544, 31 USPQ2d at 1557.

Accordingly, Appellants respectfully submit that claim 1 pertains to an apparatus having "*specific structural limitations*", and is therefore statutory.

(c) Thirdly, Appellants respectfully submit that claim 1 is limited to a practical application, and is therefore statutory.

Claim 1 is limited to the practical application of a function unit of the claimed apparatus to perform the claimed conversion, "***responsive to a control signal***" (e.g., an instruction). Accordingly, claim 1 does not attempt to protect or preempt all possible uses the claimed conversion. Rather, claim 1 makes it clear that the claimed conversion is performed responsive to the control signal. Accordingly, claim 1 certainly does not pertain to an invention that merely manipulates an abstract idea or solves a purely mathematical problem without any limitation to a practical application.

An invention that does not attempt to protect all uses of an algorithm is eligible for patent protection. See e.g., *In re* Deutsch, 553 F.2d 689, 193 USPQ 645 (C.C.P.A.) 1977).

Accordingly, Appellants respectfully submit that claim 1 is limited to a practical application, and is therefore statutory.

For at least one or more of these reasons, Appellants respectfully submit that claim 1 is statutory.

Appellants respectfully submit that claim 15 is statutory for one or more similar reasons.

GROUP II: CLAIMS 20-25

Claim 20 pertains to a method comprising:

"*a module fetching a first instruction that specifies a location of a first format value in a first format among a plurality of first format values of a packed data, the first format value having a plurality of sub elements each sub element having a first number of bits;*

a functional unit processing the first format value by converting the first format value to a first plurality of second format values in a second format, each of the first plurality of second format values having second format and corresponding to one of the plurality of sub elements, the second format having a multiple of the first number of bits;

storing the first plurality of second format values into a first register."

(a) Firstly, Appellants respectfully submit that claim 20 produces a useful, concrete, and tangible result, and is therefore statutory.

On page 3 of the Office Action mailed 4/12/2007, the Examiner has admitted that the result "*would appear to be **concrete** and **tangible** in the context of the claim*". Appellants respectfully agree.

However, the Examiner has asserted that "*the **useful** result appears lacking*". See e.g., page 3 of the Office Action mailed 4/12/2007. Appellants respectfully disagree. Claim 20 does produce a useful result.

Examples of uses of the result produced by claim 20 include, but are not limited to, pixel processing, providing shorter and in some case more rapidly executed code for some sequences, and signal processing scenarios. The discussion above is pertinent to this point. For brevity, this discussion will not be repeated.

For at least one or more of these reasons, Appellants respectfully submit that claim 20 produces a useful, concrete, and tangible result, and is therefore statutory.

(b) Secondly, Appellants respectfully submit that claim 20 is limited to a practical application, and is therefore statutory.

Claim 20 is limited to the practical application of implementing the method using "*a first instruction that specifies a location of a first format value in a first format among a plurality of first format values of a packed data*". Accordingly, claim 20 does not attempt to protect or preempt all possible uses the claimed conversion. Rather, claim 20 makes it clear that the method includes fetching the first instruction.

An invention that does not attempt to protect all uses of an algorithm is eligible for patent protection. See e.g., *In re* Deutsch, 553 F.2d 689, 193 USPQ 645 (C.C.P.A.) 1977).

Accordingly, Appellants respectfully submit that claim 20 is limited to a practical application, and is therefore statutory.

For at least one or more of these reasons, Appellants respectfully submit that claim 20 is statutory.

GROUP III: CLAIMS 32-33

Claim 32 pertains to:

"A tangible machine readable medium carrying an instruction, which if executed by a machine, causes the machine to perform the operations of:

converting an integer value, the integer value being among a plurality of integer values of a packed data and having a first integer format having a plurality of sub elements each having a first number of bits, to a plurality of floating point values, each of the plurality of floating point values having a first floating point format, the first floating point format having a multiple of the first number of bits;

storing the plurality of floating point values into a first register."

(a) Firstly, Appellants respectfully submit that claim 32 produces a useful, concrete, and tangible result, and is therefore statutory.

On page 3 of the Office Action mailed 4/12/2007, the Examiner has admitted that the result "*would appear to be **concrete** and **tangible** in the context of the claim*". Appellants respectfully agree.

However, the Examiner has asserted that "*the **useful** result appears lacking*". See e.g., page 3 of the Office Action mailed 4/12/2007. Appellants respectfully disagree. Claim 32 does produce a useful result.

Examples of uses of the result produced by claim 32 include, but are not limited to, pixel processing, providing shorter and in some case more rapidly executed code for some sequences, and signal processing scenarios. The discussion above is pertinent to this point. For brevity, this discussion will not be repeated.

For at least one or more of these reasons, Appellants respectfully submit that claim 32 produces a useful, concrete, and tangible result, and is therefore statutory.

(b) Secondly, Appellants respectfully submit that claim 32 pertains to a "tangible machine-readable medium carrying an instruction", and is therefore statutory.

As understood by Appellants, computer programs embodied in a tangible medium are patentable subject matter under 35 U.S.C. Section 101. As discussed in MPEP 2106.01, "*When functional descriptive material is recorded on some computer-readable medium, it becomes structurally and functionally interrelated to the medium and will be statutory in most cases (emphasis added) since use of technology permits the function of the descriptive material to be realized*". As discussed in MPEP 2106.01 I., "*a claimed computer-readible medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory*" (emphasis added). See e.g., Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035. See also e.g., *In re* Beauregard, 35 USPQ 2d 1383, 1384 (Fed. Cir. 1995).

(c) Thirdly, Appellants respectfully submit that claim 32 is limited to a practical application, and is therefore statutory.

Claim 32 is limited to the practical application of performing the claimed operations as a result of the machine executing the instruction. Accordingly, claim 32 does not attempt to

protect or preempt all possible uses of the claimed operations. Rather, claim 32 makes it clear that the claimed operations are performed as a result of the machine executing the instruction.

An invention that does not attempt to protect all uses of an algorithm is eligible for patent protection. See e.g., *In re* Deutsch, 553 F.2d 689, 193 USPQ 645 (C.C.P.A.) 1977).

Accordingly, Appellants respectfully submit that claim 32 is limited to a practical application, and is therefore statutory.

For at least one or more of these reasons, Appellants respectfully submit that claim 32 is statutory.

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CONCLUSION

Based on the foregoing, Appellants request that the Board overturn the rejection of all pending claims and hold that all of the claims of the present application are allowable.

Appellants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Please charge any shortages and credit any overpayment to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 9/10/07 By Brent E. Vecchia

Brent E. Vecchia, Reg. No. 48,011
Tel.: (303) 740-1980 (Mountain Time)

1279 Oakmead Parkway
Sunnyvale, California 94085-4040

VIII. CLAIMS APPENDIX (37 C.F.R. § 41.37(c)(1)(viii))

The text of the claims involved in the appeal are:

1. (Previously Presented) An apparatus comprising:

a destination storage location corresponding to a first architectural register;

a functional unit to process a packed format values by converting, responsive to a control signal, a first packed first format value in a first format selected from a first plurality of packed first format values in the first format to a first plurality of second format values, said first packed first format value having a plurality of sub elements each having a first number of bits, each of the first plurality of second format values being a number represented in a second format and having a second number of bits which is greater than the first number of bits, said functional unit to store all of said first plurality of second format values into said first architectural register.

2. (Original) The apparatus of claim 1 wherein the second number of bits is a power-of-two multiple of the first number of bits.

3. (Original) The apparatus of claim 2 wherein a source specifier is to specify either a second architectural register or a memory location as a source storage location and further wherein a destination specifier is to specify the first architectural register as the destination storage location.

4. (Original) The apparatus of claim 3 wherein said first format is an integer format and wherein said second format is a floating point format.

5. (Original) The apparatus of claim 4 further comprising:

a decoder to receive a single convert instruction, said decoder to generate said control signal in response to the single convert instruction.

6. (Original) The apparatus of claim 1 wherein said functional unit chooses one of said first plurality of packed first format values to convert based on an immediate operand value.

7. (Original) The apparatus of claim 5 wherein an opcode portion of said single convert instruction specifies which of said first plurality of packed first format values to convert.

8. (Original) The apparatus of claim 5 wherein said control signal comprises a micro operation generated by the decoder in response to the single convert instruction.

9. (Original) The apparatus of claim 5 further comprising a register renaming circuit, wherein said source storage location and said destination storage location are physical registers that each have a correspondence to an architectural register, said correspondence being tracked by the register renaming circuit.

10. (Original) The apparatus of claim 9 wherein said single convert instruction comprises an opcode and an operand specifier, wherein the operand specifier is in a MOD R/M format.

11. (Original) The apparatus of claim 9 wherein said first plurality of packed first format values are N bit integer values and wherein said first packed first format value is an N bit integer value, wherein said plurality of sub elements is M sub elements and wherein each of the M sub elements has N/M bits, and further wherein each of the first plurality of second format values is an N-bit floating point result.

12. (Original) The apparatus of claim 1 further comprising a second destination storage location, wherein said functional unit is further responsive to a second control signal to convert a second plurality of second format values in the second format having the second number of bits to a second first format value and to store the second first format value in one of a plurality of

packed first format value positions in said second destination storage location, wherein said second first format value comprises saturated representations of the second plurality of second format values in the first format.

13. (Original) The apparatus of claim 3 wherein said first architectural register and said second architectural register are part of a first group of architectural registers, the first group of architectural registers having a first size.

14. (Original) The apparatus of claim 12 wherein first architectural register and said second destination storage location are registers in a group of xmm registers.

15. (Previously Presented) An apparatus comprising:

a decoder to receive a first instruction and to decode said first instruction into a control signal;

a functional unit coupled to the decoder to receive the control signal, the functional unit to responsively process a plurality of floating point values value by converting convert a first plurality of floating point values in a first floating point format having a first number of bits into a first integer value comprising a plurality of sub elements each having a second number of bits less than the first number of bits and to store said first integer value in a first position in a first register, the first register being capable of storing a plurality of integer values in a plurality of individually accessible positions.

16. (Original) The apparatus of claim 15 wherein said first instruction comprises an opcode, a first operand specifier, an immediate operand, and a second operand specifier, wherein the first operand specifier specifies a source from which the functional unit is to retrieve the first plurality of floating point numbers, the second operand specifier specifies the first register from a plurality of registers, and wherein the immediate operand specifies one of a plurality of locations in the first register in which the first integer value is to be stored.

17. (Original) The apparatus of claim 16 wherein said decoder is to decode a second instruction and to responsively generate a second signal, and wherein said functional unit, responsive to said second signal, is to convert a second integer value to a second plurality of floating point values in the first floating point format and to store said second plurality of floating point values into a second register.

18. (Original) The apparatus of claim 17 wherein said first register and said second register are part of a first group of architectural registers, and further wherein said plurality of sub elements comprise saturated representations of said first plurality of floating point values.

19. (Original) The apparatus of claim 18 wherein a second immediate operand is to specify one location of a second plurality of locations within a register from which to retrieve the second integer value.

20. (Previously Presented) A method comprising:

a module fetching a first instruction that specifies a location of a first format value in a first format among a plurality of first format values of a packed data, the first format value having a plurality of sub elements each sub element having a first number of bits;

a functional unit processing the first format value by converting the first format value to a first plurality of second format values in a second format, each of the first plurality of second format values having second format and corresponding to one of the plurality of sub elements, the second format having a multiple of the first number of bits;

storing the first plurality of second format values into a first register.

21. (Original) The method of claim 20 wherein said location is a second register, wherein said first register and said second register are registers in a single group of architectural registers.

22. (Original) The method of claim 21 further comprising:

fetching a second instruction that specifies a second location of a second plurality of second format values in the second format;

converting the second plurality of second format values to a second first format value;

storing the second first format value in a third register, wherein the third register is also in the single group of architectural registers.

23. (Original) The method of claim 22 further comprising:

specifying which of the plurality of first format values to convert by an immediate operand;

specifying one a plurality of destination packed data positions for the second first format value with a second immediate operand.

24. (Original) The method of claim 22 wherein said first format is an integer format and wherein said second format is a floating point format.

25. (Original) The method of claim 24 further comprising:

saturating each of the second plurality of second format values to generate a plurality of clamped sub elements of the second first format value.

26. (Original) A system comprising:

a memory to store a first instruction and an image processing sequence that operates on image data in a second format;

a processor coupled to the memory to process a first operand comprising a plurality of packed integer data values according to the first instruction by converting one of the plurality of packed integer data values into a first plurality of values in a second format and to store said first plurality of values in the second format into a register corresponding to an architectural register,

said first plurality of values in the second format being manipulated as part of an image by said image processing sequence;

a graphics interface coupled to the processor to receive graphical data representative of the image from said processor;

a display to display said image.

27. (Original) The system of claim 26 wherein said first plurality of values in said second format have a larger total number of bits than said one of said plurality of packed integer data values.

28. (Original) The system of claim 26 wherein said memory stores a second instruction to cause the processor to convert a second plurality of values in the second format which are a result of manipulation of said first plurality of values in the second format by said image processing sequence into a second integer data value and to store the second integer data value to a second register corresponding to a second architectural register, and further wherein said second integer data value is written to the graphics interface as a pixel value.

29. (Original) The system of claim 28 wherein said first instruction is a first convert instruction, wherein each of the plurality of packed integer data values has a plurality of sub elements each having a first number of bits and wherein each of the first plurality of values corresponds to one of the plurality of sub elements and has a first floating point format having a multiple of the first number of bits.

30. (Original) The system of claim 26 wherein said first instruction specifies a first one of the plurality of packed integer data values, and wherein said plurality of packed integer data values comprises N integer data values, wherein the memory stores N convert instructions including the first instruction to convert the N integer data values into a set of N pluralities of floating point values.

31. (Original) The system of claim 30 wherein said image processing sequence is to operate on said set of N pluralities of floating point values to generate a second N pluralities of floating point values as a portion of the image, and further wherein said memory stores a second plurality of N convert instructions to convert each of second N pluralities of floating point values back to integer data values in a packed format.

32. (Previously Presented) A tangible machine readable medium carrying an instruction, which if executed by a machine, causes the machine to perform the operations of:

converting an integer value, the integer value being among a plurality of integer values of a packed data and having a first integer format having a plurality of sub elements each having a first number of bits, to a plurality of floating point values; each of the plurality of floating point values having a first floating point format, the first floating point format having a multiple of the first number of bits;

storing the plurality of floating point values into a first register.

33. (Original) The machine readable medium of claim 32, wherein said machine readable medium further stores one or more additional instructions, which if executed by the machine, cause the machine to perform:

converting a second plurality of floating point values in the first floating point format to a second integer value in the first integer format;

storing the second integer value in a third register, wherein the third register is also in the group of architectural registers and is capable of storing a plurality of integer values in the first integer format.

IX. EVIDENCE APPENDIX (37 C.F.R. § 41.37(c)(1)(ix))

To the best of Appellant's knowledge, no evidence has been submitted pursuant to 37 CFR Sections 1.130, 1.131, or 1.132.

X. RELATED PROCEEDINGS APPENDIX (37 C.F.R. § 41.37(c)(1)(x))

(To the best of Appellant's knowledge, there are no related appeals or interferences.)